Design three-level converter as super capacitor interface for EV hybrid energy storage system

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Abstract: The super capacitor (SC) battery hybrid energy storage system (HESS) can be widely used as the energy bank with lots of advantages. Optimized topologies and high-efficiency converters are necessary as the power interface of SC bank for different applications. In this paper, the converter prototype with three-level (TL) topology is applied as SC power interface, which is designed to link low- voltage DC bus with bidirectional high current output ability for electric vehicles (EV) application. The comparative analysis of components size and converter loss is made based on the experiments among different converter topologies, which shows the effectiveness of three-level converter in our application. The control principle and action modes of three-level converter are introduced. Two aspects of converter control design, the response of output current control loop and the voltage balance between the two SC banks in three-level topology, will be considered in the following step.

Key Words: hybrid energy storage system; super capacitor; three-level converter; converter control

1. INTRODUCTION

The hybrid energy storage system is generally composed of different energy sources, such as batteries and SC, which enable to provide both the permanent and transient powers demanded by the load.
So HESS can be applied in many aspects, such as electric vehicles. Many hybrid topologies are researched for different requirements, including serial, passive cascaded, semi-active structure and so on.

For small scaled EV application, the power train requirement is usually less than 10kw, and the main DC bus voltage is below 200V. The main energy storage device is directly linked to DC bus. There must be one DC/DC converter used as the interface between the SC bank and electric vehicle power train system. This DC/DC converter must have the characteristics as below:

- Bidirectional power flow;
- Wide variable voltage range on SC side;
- Relatively constant voltage on DC bus side;
- Wide response bandwidth of output current;
- Non-isolated structure is preferred.

As is known, conventional three-level and multi-level converters are widely used in high or ultra-high voltage application, because the limitation of the maximum voltage of power semiconductor devices. Also multi-level technology can reduce VA rate of every active component, so the switching loss of the converter can fall down.

For our hybrid electric vehicle prototype, shown in Fig.1, the requirement for SC converter is that DC voltage is below 100V and the peak output current is 100A, which is for peak power comprehension function of super capacitor [1]. Also the compact size and high conversion efficiency is the perusing objective.

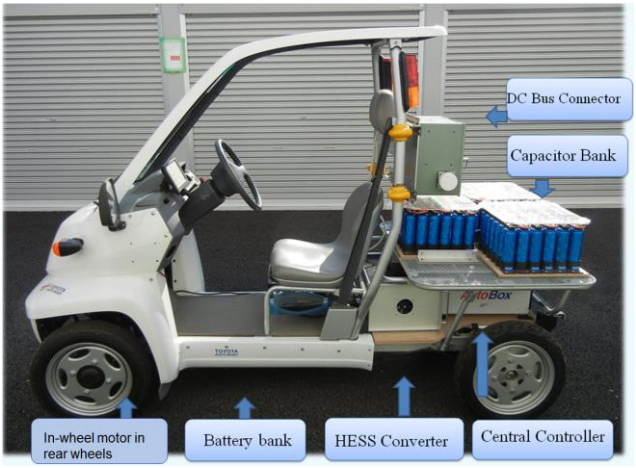


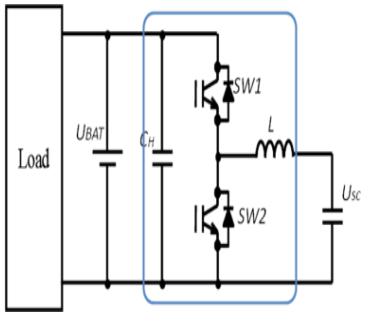
Fig. 1. Hybrid electric vehicle prototype

Table 1 Parameters of Hybrid EV Prototype

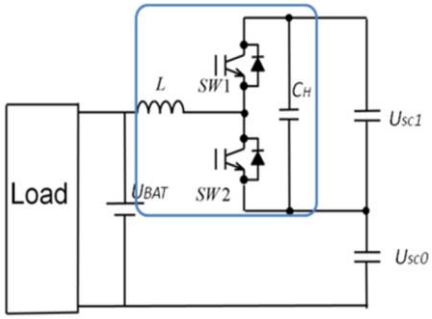
EV body	Toyota Autobody COMS
In wheel Motor	Peak power 2KW X2
Max Speed	50Km/h
Weight	430Kg
DC bus Voltage	72V
Battery Bank	Lead Acid 12V 42Ah X6
SC Bank	90V 64F module X3
DC bus converter	Peak current 100A

2. ANALYSIS OF CONVERTER PROTOTYPES AS SUPERCAPACITOR INTERFACE

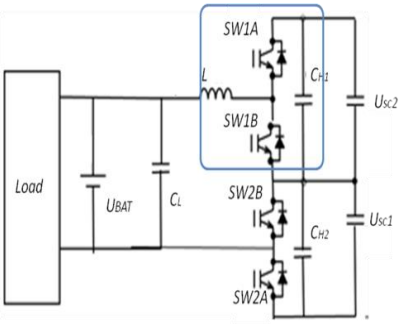
Two improved topologies are introduced here. First is the three-level converter topology for SC application as shown in Fig. 2 (b). Another topological approach first presented in our lab under the name of half-controlled (HC) converter, shown in Fig. 2 (c) [2, 3]. The aims of both improved topologies are size reduction and efficiency improvement of the power interface. Both of these two improved topologies set the SC to high voltage level to increase the efficiency. The utilization of state of charge of the SC bank should be first considered in the system design. For our design, 25% of SoC remains after every deep discharge for SC bank is acceptable, considering the size of SC energy bank and the SC modules protection.



(a) Bidirectional half-bridge (HB) converter



(b) Three-level (TL) converter



(c) Half-controlled (HC) converter

Fig. 2. Converter topologies for SC interface

Table 2 Comparison between different converters for SC

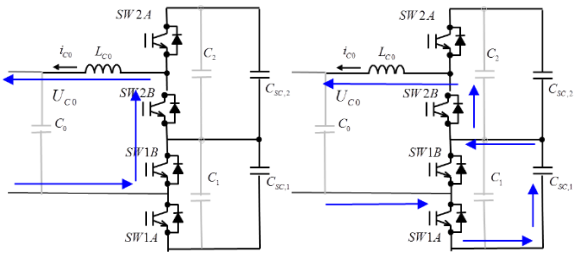
Bidirectional Converters For SC interface	Bidirectional Boost Converter	Three Level converter	Half-Controlled Converter
Operation Condition	0<Usc<UBAT	(USC1+USC2)/2 <UBAT UBAT<USC1+USC2	Usc0<UBAT UBAT<USC0+USC1
Minimum SC Storage Energy	0	> 25%SoC	25% SoC
Switching Elements	2	2 (+ 2)	4
Designed Inductance Size	100%	50%	25%
SC banks Voltages balance	No	Need	Need

The comparison among different converters for SC interface is given in Table 2. .

From the analysis of half-controlled converter, we can naturally deduce that, the super capacitor energy bank can be separated to different banks inside the topology. The fundamental reason is that, the rated voltage of the super capacitor cell is determined by the voltage of the electrolyte. The typical cell voltage is 1–2.8 V, depending on the electrolyte technology [4]. In order to obtain a higher working voltage that is determined by the application, elementary cells are series connected into one capacitor module.

The three-level converter uses four switching elements for the output power from SC [5]. The upper group switch has 180 degree phase error with the lower group. Consequently, the switching frequency of the whole chopper system is twice as the chopper using two switch elements. Naturally, if the requirement of the output ripple is the same, the inductance can be decreased to 25%, compared to the conventional design. Therefore three-level converter can remarkably reduce the output current ripple for the high current output situation for EV powertrain system. The disadvantage is that the number of switching elements is increased. While within low voltage condition，the inductance cost is the main part comparing with the switch power devices.

3. OPERATION PRINCIPLE OF THREE-LEVEL CONVERTER AS SUPER CAPACITOR INTERFACE



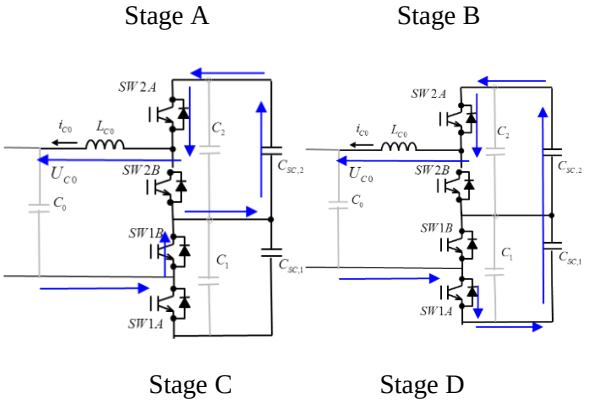


Fig. 3. Different stages of TL converter as SC power interface in one action period

Three-level converters are a well-adopted solution in applications with high input voltage and high switching frequency [5, 6]. The voltage stress of the switches is only half of the total dc bus voltage. This allows us to use lower-voltage-rated switches and still having better switching and conduction performance compared to the switches rated on the full blocking voltage. Therefore, the converter cost and efficiency can be significantly improved compared to two-level converters, such as half-bridge and Cuk converter, particularly when the switching frequency is above 20 kHz.

The three-level converter topology for SC application is shown in Fig. 3. It is different than conventional three-level converter application, because the two SC banks is linked directly to the two group choppers, and the transient response of SC banks voltage is nearly close to constant power sources

The capacitors are series connected and serve as a capacitive voltage divider to split the dc bus voltage SC_{12} into two equal voltages SC_1 and SC_2, when considering the basic condition that the two separated super capacitor bank is strictly equal with the same filter capacitor linked to the chopper.

As shown in Fig. 4, the states of the switches SW1B and SW1A are determined by a switching function s_1 and the complementary function, while the states of switches SW2B and SW2A are determined by a switching function s_2 and the complementary function. The switching functions s_1 and s_2 are generated by pulse width modulators PWM1 and PWM2. The phase between the triangle signal for the PWM 1 and PWM 2 will be 180 degree.

It is easy to calculate the peak to peak current ripple.

$$\Delta i_{C0}(d)=\begin{cases}\dfrac{u_{C12}}{L_{C0}2f_{sw}}(1-2d)d & \mathrm{d}\le 0.5\\ \dfrac{u_{C12}}{L_{C0}2f_{sw}}(2d-1)(1-d) & \mathrm{d}\ge 0.5\end{cases} \quad (1)$$

$$\Delta i_{C0\max}=\frac{u_{C12}}{16L_{C0}f_{sw}} \quad (2)$$

The inductance size is 1/4 of that for the half-bridge dc–dc converter for the same current ripple and the same switching frequency [5].

4. CONTROL ASPECTS OF THREE-LEVEL CONVERTER FOR SC INTERFACE

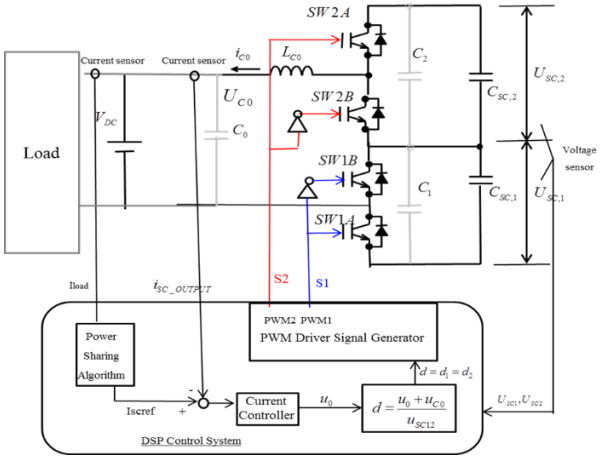


Fig. 4. Converter topologies and current control for SC interface to HESS

The aim of this improved topologies for SC interface, is size reduction and efficiency improvement of the power interface, special in the SC bank high voltage condition. The inductance is 25% of the inductance of the half-bridge dc–dc converter for the same current ripple and the same switching frequency. In the other hand, the application of TL converter high voltage side as the SC interface, the operation condition will be $u_{C0}\le u_{C1}+u_{C2}$. The SoC of the SC bank can be used from 25% to 100%, which is acceptable when SC modules frequently charge and discharge.

From the conclusion of the previous research, shown in Fig. 5, the transfer function of input voltage and output current will be:

$$G_{i_{c0}u_0}=\frac{i_{C0}}{u_0}=\frac{1}{sL_{C0}+R_{LC0}} \quad (3)$$

It means that, considering only the current control loop,

if the voltage signals U_{SC1} and U_{SC2} are measurable by voltage sensors and can be fed back in real-time. The current control system can be transferred to one order system.

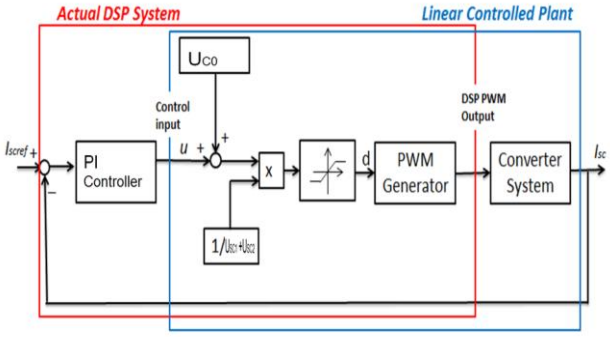


Fig. 5. Current control block for TL converter

PI controller is designed as current controller, the system open loop transfer function is

$$\frac{I(s)}{I_{ref}(s)} = \frac{K_P K_I s + 1}{K_I s(L_{C0} + R_{LC0} s)} \tag{4}$$

The current controller can be designed using the classic linear control method without small signal operation.

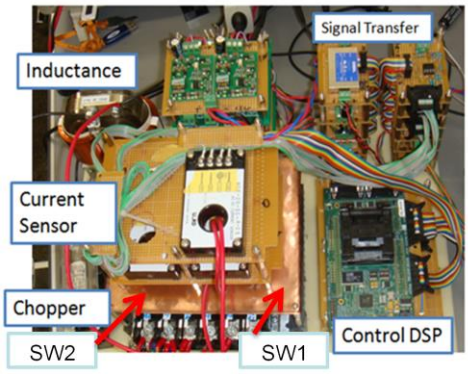


Fig. 6. First version of three-level converter prototype

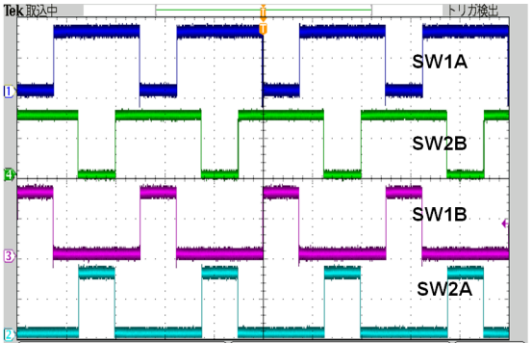


Fig. 7. Control signals of three-level converter

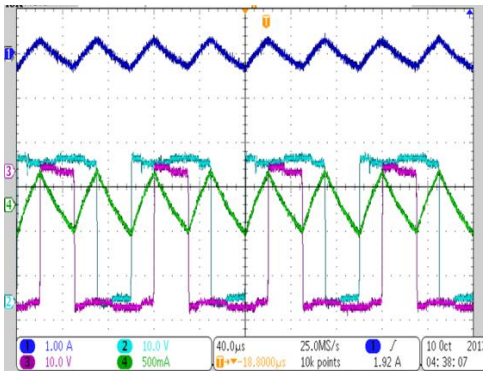


Fig. 8. Switch actions and output current of three-level converter prototype

Fig.7 and Fig.8 shows the action of three-level converter prototype designed for super capacitor bank interface. The test voltage of SC_1 and SC_2 is 30 V respectively.

The pink signal shows the voltage in switch SW1B, and the blue signal shows the voltage hold by SW2B. Green current signal means output current $i_{C0.}$ In the condition as shown in Fig. 8， the average output current is equal to 0， when

$$(u_{C1} + u_{C2})d = u_{C0} \tag{5}$$

The ripple of the output current is nearly 0.75A， which is the same as the calculation result based on Equation (2) .

5. THE FOLLOWING STEPS

In the next step, the dynamic characteristic of SC bank charging/discharging process will be analyzed. In order to confirm the power output performance of SC bank, a simple RC model of SC with the nonlinear section will be applied. Two aspects of converter control are considered in the controller parameters tuning in the next step: the response of output current control loop and the voltage balance between two SC banks in three-level topology. The output current response time is important for our converter interface, because the super capacitor banks works as high-frequency power provider for the power train system. The following is about the experiment system setup and the test environment. The comparative analysis of components size and converter loss will be made, among three-level converter, interleaved converter, and common buck/boost converter for high current solution. The experiment and power analysis results will be made to show three- level topology is one optimized solution as super capacitor interface in our application case.

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